REMARKS

The applicant has amended claims 1, 9, 10, 12, 13, 18, and 20, and added new claims 27 and 28. The amendments are supported by page 7, lines 6 to 23 of the specification.

Below, the applicant's comments are preceded by related remarks of the examiner set forth in small bold font.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "130" has been used to designate both an Interface Bus and a Merge Engine in Figure 1.

3. The disclosure is objected to because of the following informalities: On Page 4, line 23 and Page 5, line 4, when referring to figure 1, reference number 130 is described as representing two different features of the invention. On Page 4, reference number 130 refers to a Merge Engine while on Page 5 reference number 130 refers to an interface bus.

The applicant has amended the drawings and specification so that reference "130" is used to designate an interface bus and reference "134" is used to designate a merge engine.

5. Claims 1-6, 8-10, 13-19, and 21-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Glew et al. (5,561,780).

Regarding claims 1-6, and 10, Glew et al. teaches a buffer 132 ("cache") with a number of cache-line sized storage locations 136 ("cache lines") and an eviction unit 139 enabled to evict data from the storage locations when partial writes fill a single storage location one storage portion 140 ("cache line has multiple portions") at a time. A thirty-two-byte validity 144 ("validity bit storage") keeps track of which of the thirty-two portions of each storage location has been written to and when all are full, the storage location ("cache line") is evicted (See Figure 4 and Column 4, lines 59-67 and Column 7, lines l-30). Glew et al. also discloses that storage in the buffer 132 is very much like storage on an on-chip cache unit (DCU), therefore, as DCU's, buffer 132 may store data corresponding to locations in main memory (see Column 1, lines 25-38 and Column 7, lines 30-32).

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Regarding Claims 13, 15, 18 and 22-26, Glew et al. teaches a buffer 132 ("cache") with a number of cache-line sized storage locations 136 ("cache lines") being written to through the use of a write combining unit 138, and an eviction unit 139 enabled to evict data from the storage locations when partial writes fill a single storage location one storage portion 140 ("cache line has multiple portions") at a time. A thirty-two-byte validity field 144 ("validity bit storage") keeps track of which of the thirty-two portions of each storage location has been written to and when all are full, the storage location ("cache line")is evicted (See Figure 4 and Column 4, lines 59-67 and Column 7, lines l-30). Glew et al. also discloses that storage in the buffer 132 is very much like storage on an on-chip cache unit (DCU), therefore, as DCU's, buffer 132 may store data corresponding to locations in main memory (See Column 1, lines 25-38 and Column 7, lines 30-32).

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7. Claims 11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glew et al. (5,561,780).

8. Claims 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glew et al. (5,561,780) as applied to claims 11 and 18 respectively, and further in view of "The Cache Memory Book" by Jim Handy. Glew et al. teaches the invention as set forth by claims 11 and 18 above. Glew et al. does not teach buffer 132 being part of a coherency protocol. Handy teaches cache coherency which prevents stale data from being confused with current data (page 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the cache coherency of Handy to the buffer of Glew et al. since this buffer behaves much like a cache and adding such protocol would prevent the confusion between good and useless data.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glew et al. (5,561,780) in view of Van Huben et al. (2002/0083243 Al).

The examiner acknowledges that Glew does not teach a buffer being part of a coherency protocol. The examiner points to Handy as providing what is missing in Glew. The applicant submits that the combination of Glew and Handy would not have made obvious "a cache memory comprising cache lines to store data, the cache memory complying with a cache coherency protocol; and an eviction mechanism to evict data stored in one of the cache lines based on validity state information," as recited in amended claim 1.

Glew discloses a "cache-line-sized write buffer line" in which a plurality of uncacheable data units are combined. In Glew, to implement the cache-line-sized write buffer, "processor ordering requirements are ignored and global observability requirements are relaxed. In particular, when the buffer line is evicted using partial writes, no substantial delay is provided between consecutive partial writes, which are typically needed if global observability must be provided." (col. 5, lines 4-13) Thus, Glew actually teaches away from using a cache memory that complies with a cache coherent protocol. There would be no incentive to combine Glew with Handy. Thus, claim 1 is patentable.

Claims 2-21 are patentable for at least the same reasons as claim 1.

With respect to claim 22, Glew and Handy, independently or in combination, do not disclose or suggest "initiating write transactions by an input/output device to write data; writing the data into a cache memory; evicting the data from the cache memory; and writing the data into a main memory," as recited in the claim. In Glew, the write transactions (in which write data is stored in a cache memory) are initiated by a microprocessor (such as 110 of FIG. 3), not by an

input/output device (e.g., 25 of FIG. 3). Glew does not disclose or suggest that data from an input/output device be written into a cache memory before being written into a main memory.

Claims 23-26 are patentable for at least the same reasons as claim 22.

Enclosed is a $36 check for excess claim fees. Please apply any other charges or credits to deposit account 06-1050, referencing attorney docket 10559-639001.

Respectfully submitted,

Date: Nov. 10, 2003

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* See attached document certifying that Rex Huang has limited recognition to practice before the U.S. Patent and Trademark Office under 37 C.F.R. § 10.9(b).

ANNOTATED SHEET SHOWING CHANGES

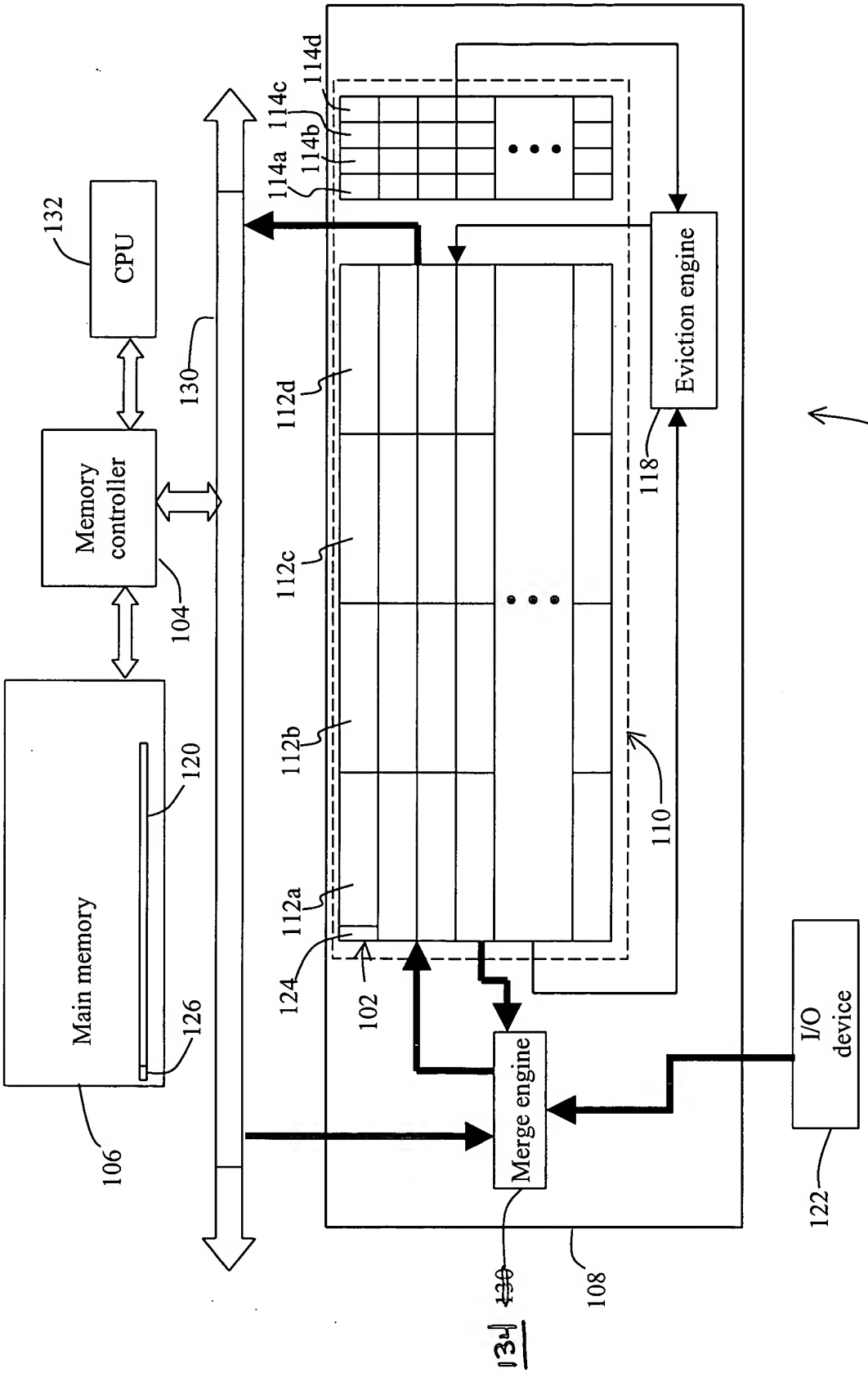

Figure 1

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Expires: May 16, 2004

Harry I. Moatz
Director of Enrollment and Discipline